Six Sample CS130 Waiver Test Questions

No references are allowed except an 8086 assembly language reference manual. No internet or cell phones allowed.

1. You just completed a huge system project and feel great that it is finished. Then your manager comes by and says, we have some new sources of data to process and you have to incorporate this capability into your project. You really want to say “NO we can't do it”. You tell the manager that we have run out of hardware interrupt signals, and you hope your manager believes you. However, being your manager, he knows of a way. He tells you there are four new hardware interrupts and he knows that you can logically OR these new signals with an existing interrupt signal together making any of the five sources cause a processor interrupt to occur.

What would you have to do to modify your existing interrupt service routine (the one that serviced the original interrupt, subsequently OR-ed with the new four sources) in order to handle any of the other OR-ed interrupt sources? There are two broad categories of possibilities. Also note that your manager will allow you to add an external register (external to the CPU) to your system that copies the state of these five interrupt lines at the point in time when one of these interrupts went active.

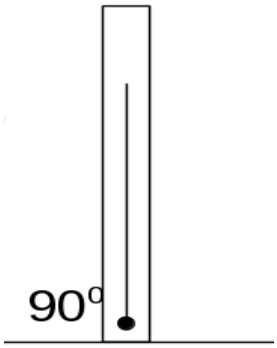
(I am not asking for the code, but the general modification. It can be explained in a few sentences.)

2. Why must there be cache coherency on a multi-core CPU or a multiple CPU system?

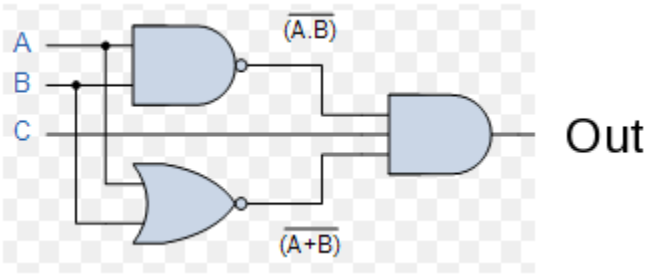
3. Write an 8086 assembly routine (just the code) that will continuously read data bytes from address offset [1000H]. At [1000H] you are reading in the angle of a pole that is positioned on a pin.

If you read 90H, the pole is vertical. If you read less than 90H, the pole is leaning to the left. If you read more than 90H the pole is leaning to the right.

Your goal is to keep the pole vertical by continuously sending an error value to address offset [2000]. If the pole is leaning to the left (reading less than 90H) you need to write the error value to [2000] and 0H to address offset [2001]. If the pole is leaning to the right write the error value to [2000] and write a 1H to address offset [2001].

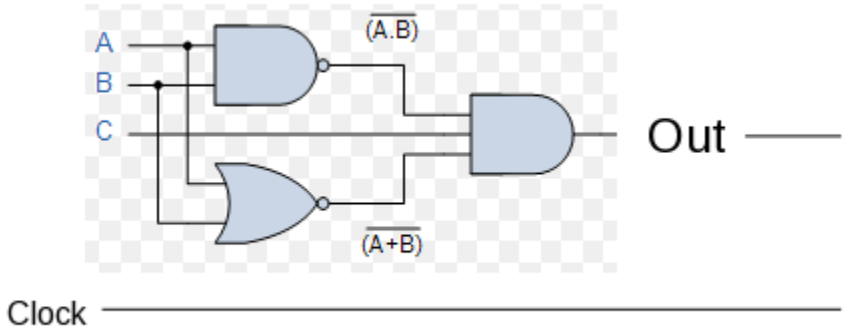


4a) Generate the truth table for the following simple circuit:



C	B	A	Out

4b) Given this same circuit add a single item used in sequential logic to gate Out with the falling edge of a clock, making a new clock-gated Out.



5) Write an x86 assembly language that corresponds with the following comments:

```
                                    ; setup stack pointer at 1034H
                                    ; setup three variables in DSEG
                                    ; Var1 which is a byte initialized to 2
                                    ; Var2 which is a byte initialized to 80H
                                    ; Var3 which is an uninitialized 16 bit word
                                    ; start code
                                    ; setup DSEG to point to .data
                                    ; clear the AH register
                                    ; and copy current value of Var1 into AL
                                    ; use CL as a shift counter
                                    ; rotate AX right Var2 times
                                    ; and copy the rotated AX in Var3
INT 3                               ; exit
```

6) Your new IT startup has won a contract with a customer who needs a storage system re-architecture. Your customer has a hacked together a Storage Area Network (FC SAN) for years with storage in their building as well as multiple facilities next door and several kilometers distance. The storage appears to be nearly broke down due to age and the person who put it all together has left the company. Your customer is a rapidly expanding company, but doesn't want to store their proprietary data on any commercial cloud. What would be the type of storage architecture you would push with your customer and why?

These samples were submitted by CSE Lecturer, David Davidian, September 2, 2017